

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE



Membership Publications/Services Standards Conferences Careers/Jobs

**IEEE Xplore®**  
 RELEASE 1.7

 Welcome  
 United States Patent and Trademark Office

[Help](#) [FAQ](#) [Terms](#) [IEEE Peer Review](#)
[Quick Links](#)

Welcome to IEEE Xplore®

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

## Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

## Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced

## Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

Print Format

Your search matched **10** of **1037503** documents.  
 A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

**Refine This Search:**

You may refine your search by editing the current search expression or enter a new one in the text box.

bdd based symbolic

☐ Check to search within this result set
**Results Key:**
**JNL** = Journal or Magazine   **CNF** = Conference   **STD** = Standard
**1 Decomposed symbolic forward traversals of large finite state machi**
*Quer, S.; Cabodi, G.; Camurati, P.;*

Design Automation Conference, 1996, with EURO-VHDL '96 and Exhibition, Proceedings EURO-DAC '96, European , 16-20 Sept. 1996

Pages:170 - 175

[\[Abstract\]](#)   [\[PDF Full-Text \(564 KB\)\]](#)   IEEE CNF
**2 Dynamic scheduling and clustering in symbolic image computation**
*Cabodi, G.; Camurati, P.; Quer, S.;*

Design, Automation and Test in Europe Conference and Exhibition, 2002. Proceedings , 4-8 March 2002

Pages:150 - 156

[\[Abstract\]](#)   [\[PDF Full-Text \(333 KB\)\]](#)   IEEE CNF
**3 Reliability evaluation of combinational logic circuits by symbolic simulation**
*Bogliolo, A.; Damiani, M.; Olivo, P.; Ricco, B.;*

VLSI Test Symposium, 1995. Proceedings., 13th IEEE , 30 April-3 May 1995

Pages:235 - 242

[\[Abstract\]](#)   [\[PDF Full-Text \(652 KB\)\]](#)   IEEE CNF
**4 Accurate logic-level power estimation**
*Bogliolo, A.; Ricco, B.; Benini, L.; De Micheli, G.;*

Low Power Electronics, 1995., IEEE Symposium on , 9-11 Oct. 1995

Pages:40 - 41

[\[Abstract\]](#)   [\[PDF Full-Text \(212 KB\)\]](#)   IEEE CNF

---

**5 Efficient state classification of finite-state Markov chains***Aiguo Xie; Beerel, P.A.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on , Volume: 17 , Issue: 12 , Dec. 1998

Pages:1334 - 1339

[\[Abstract\]](#)   [\[PDF Full-Text \(192 KB\)\]](#)   IEEE JNL

---

**6 Counterexample-guided choice of projections in approximate symbolic model checking***Govindaraju, S.G.; Dill, D.L.;*

Computer Aided Design, 2000. ICCAD-2000. IEEE/ACM International Conference on , 5-9 Nov. 2000

Pages:115 - 119

[\[Abstract\]](#)   [\[PDF Full-Text \(448 KB\)\]](#)   IEEE CNF

---

**7 Improved reachability analysis of large finite state machines***Cabodi, G.; Camurati, P.; Quer, S.;*

Computer-Aided Design, 1996. ICCAD-96. Digest of Technical Papers., 1996 IEEE/ACM International Conference on , 10-14 Nov. 1996

Pages:354 - 360

[\[Abstract\]](#)   [\[PDF Full-Text \(620 KB\)\]](#)   IEEE CNF

---

**8 SAT-based unbounded symbolic model checking***Hyeong-Ju Kang; In-Cheol Park;*

Design Automation Conference, 2003. Proceedings , 2-6 June 2003

Pages:840 - 843

[\[Abstract\]](#)   [\[PDF Full-Text \(503 KB\)\]](#)   IEEE CNF

---

**9 Improved SAT-based bounded reachability analysis***Ganai, M.K.; Aziz, A.;*

Design Automation Conference, 2002. Proceedings of ASP-DAC 2002. 7th Asia South Pacific and the 15th International Conference on VLSI Design. Proceedings , 7-11 Jan. 2002

Pages:729 - 734

[\[Abstract\]](#)   [\[PDF Full-Text \(448 KB\)\]](#)   IEEE CNF

---

**10 Efficient state classification of finite state Markov chains***Xie, A.; Beerel, P.A.;*

Design Automation Conference, 1998. Proceedings , 15-19 June 1998

Pages:605 - 610

[\[Abstract\]](#)   [\[PDF Full-Text \(620 KB\)\]](#)   IEEE CNF